

REMARKS

Favorable reconsideration of this application is requested. Claims 1 and 3-17 are pending. Claims 2 and 14 have been canceled without prejudice or disclaimer. The revision to claims 1 and 9 is supported by original claims 2 and 14, for example. Claims 1, 3-13 and 15-17 are pending.

Claim 1 requires a pair of opposed circuit substrates with an insulating layer disposed therebetween. An inner via, which connects wiring patterns on the opposed substrates, is provided in the insulating layer. An electronic component is embedded in the insulating layer. The substrates include an insulating base material containing a resin, and the insulating layer contains an inorganic filler and a resin composition containing a thermosetting resin. The glass transition temperature of the resin contained in the insulating layer (Tg1 in claim 1) is higher by at least 10°C than the glass transition temperature of the resin of the insulating base material of the circuit substrates (Tg2 in claim 1). Independent method claim 9 includes similar features.

The requirement of the different glass transition temperatures is significant. When the insulating layer has a larger coefficient of expansion than the circuit substrate, the circuit substrates will tend to block the expansion of the insulating layer in the lateral direction as the temperature is increased. As a result, the insulating layer will tend to expand in the thickness direction. The expansion in the thickness direction can put stress on the conductive material used for the inner via connecting the opposed circuit substrates. This can result in separation of the conductive material and loss of conductivity in the inner via. The problem is particularly pronounced in a product including an electronic component embedded in the insulating layer. In such products the insulating layer must be relatively thick to accommodate the electronic component, and the relatively large thickness of the insulating layer, which corresponds to the length dimension of the inner via, results in a relatively large aspect ratio (length/diameter) for the inner via. This makes the inner via more susceptible to damage and loss of conductivity when the thickness of the insulating layer expands. The higher glass transition temperature for the resin in the composition of the insulating layer promotes the ability of that resin to expand laterally, thus alleviating the pressure exerted in the thickness direction (the longitudinal direction of inner via). The experimental results reported at pages 24-26 of the present specification and the accompanying tables and figures show how the different glass transition

temperatures required by the invention of claims 1 and 9 alleviate this problem and advantageously improve the reliability of the product, the difference of at least 10 degrees further securing the advantageous properties as discussed on page 26, lines 9-31 of the specification.

Nakatani neither discloses nor suggests the invention of claims 1 and 9. Nakatani discloses a structure in which a core layer (e.g. 105 in Fig. 1 or 404 in Fig. 4) and outer wiring board substrates (e.g. 106 in Fig. 1 or 405 in Fig. 4). Contrary to the assertion in the rejection, the reference in no way discusses any particular relationship between the Tg values of the core layer and that of the outer substrates. Neither is there anything in the specific examples, including the Tables 1-3 on which the rejection relies, that discloses or suggests the different Tg values required by claims 1 and 9.

More specifically, the reference is focuses on the properties of the core member itself. For example, claim 1 requires a particular modulus of elasticity range for the insulating material of the core layer at room temperature. Claim 2 requires that the insulating material of the core layer is formed of a plurality of thermosetting resins having different Tg values, and that the modulus of elasticity is in a particular range at room temperature. Claim 3 further defines the Tg values for the insulating material of the core layer.

Tables 1-3 are part of the examples used to illustrate the properties of the core layer, and the properties reported in these tables are for the insulating material of the core layer. The reference provides no discussion of the Tg values for the outer substrates. Nor is there any basis from the information provided in the examples to assume that the different Tg values would be met inherently. Example 1 uses an aramid film for the outer substrates. The reference fails to discuss the Tg of such the materials, but those skilled in the art realize that the Tg of such materials is quite high, over 300°C. Thus this does not satisfy the $Tg1 > Tg2$ relationship required by claims 1 and 9. In Example 2, the same materials are used for the insulating material of the core layer and the outer substrates; this clearly cannot suggest the $Tg1 > Tg2$ relationship required by claims 1 and 9. Example 3 uses a ceramic that contains glass and alumina as the main components for the outer substrate. To the extent Tg is applicable to such a material, the glass temperature of the glass serving as the mother phase would be the relevant value. The reference again does not disclose this, but this again would be known to be quite high, typically on the order of 500-700°C, and as with Example 1 is far too high to meet the requirements of claims 1


and 9. Therefore, the reference does not provide the teachings for which it is cited by the rejection and the rejection should be withdrawn.

In view of the above, Applicants request reconsideration of the application in the form of a Notice of Allowance.

Respectfully submitted,

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